Eg on changes.

MODULUS OF THE COUNTER. (MOD-n COUNTER)

Modulus of a counter: Modulus of a counter is defined as the number of states through which the counter progresses during its operation.

So, mod no. of a counter is given by the following expression,

$$\text{Mod number} = 2^n$$

where n = No. of FFs.

e.g. If $n = 2$ (No. of flip-flops)
∴ Mod of counter $= 2^n = 4$

But we can restrict the number of o/p states to any number of states with a digital combinational logic circuit to reset the flip-flop.

e.g.

Design a MOD-3 asynchronous counter by using a 2-bit ripple counter.

Soln:

The required no of states = 3,

$n = 2$.

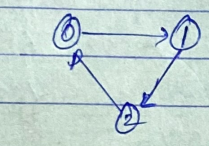
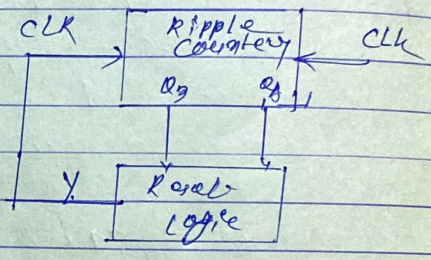


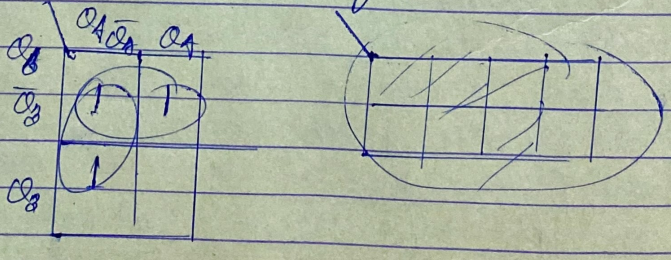
Fig: State diagram MOD-3 diagram.



Truth Table:

Flip flops outputs		output of reset logic (Y)
Q_B	Q_A	Y
0	0	1
0	1	1
1	0	1
1	1	0

Now using Truth Table we get



∴ $Y = \bar{Q}_A + \bar{Q}_B = \overline{Q_A \cdot Q_B}$.

a) circuit diagram:

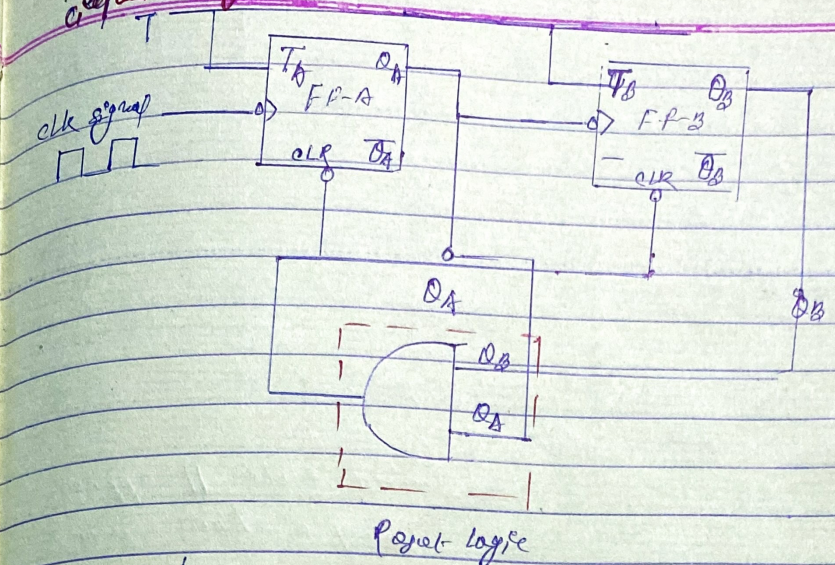


Fig: MOD-8 counter using 3 bit ripple counter.

Output frequency:- The output frequency of a Asynchronous counter is given by

$$f_0 = \frac{f_{clk}}{(MOD\text{-}Number)}$$

problems Associated with Ripple counters:

There are two major problems associated with the ripple counters

i) Generation of unwanted short duration pulse called glitch.

ii) propagation delay.

i) **Glitch:-** ⇒ Generation of unwanted short duration pulse or spike in the output of counter is called glitch.

This appears in the output of the counter with mod number 2^n.

A technical glitch for a MOD-8 counter is shown in my overleaf page.

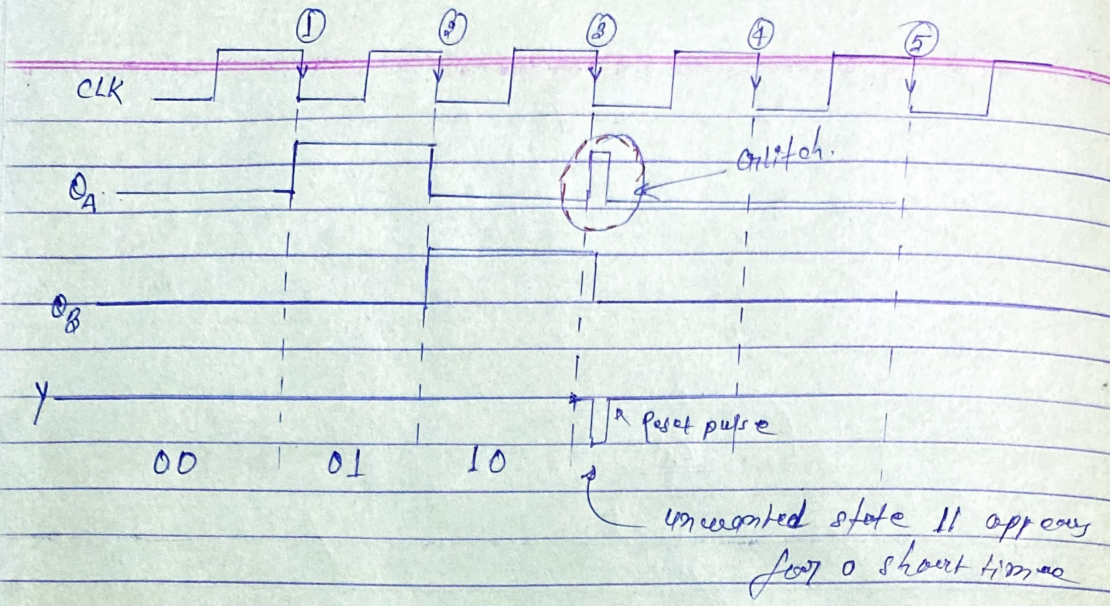


Fig: Waveforms of a MOD-3 counter.

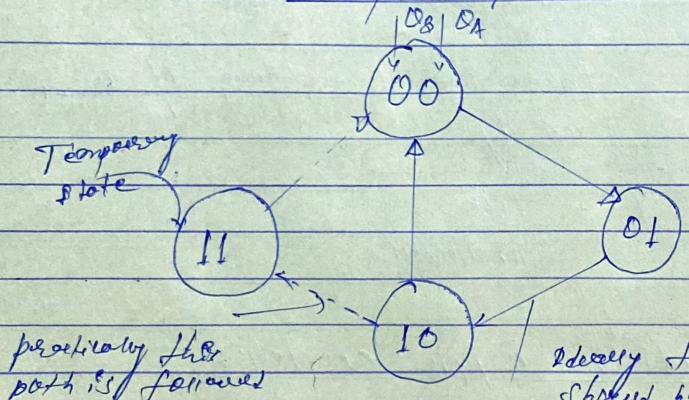


Fig: State diagram of glitch condition.

ii) The other major drawback of the ripple counter is that the propagation delay. Each FF is clocked by the transition at the output of the preceding FF. Due to the inherent propagation delay (t_{pd}) of each flip-flop, outputs of the FFs do not change simultaneously.

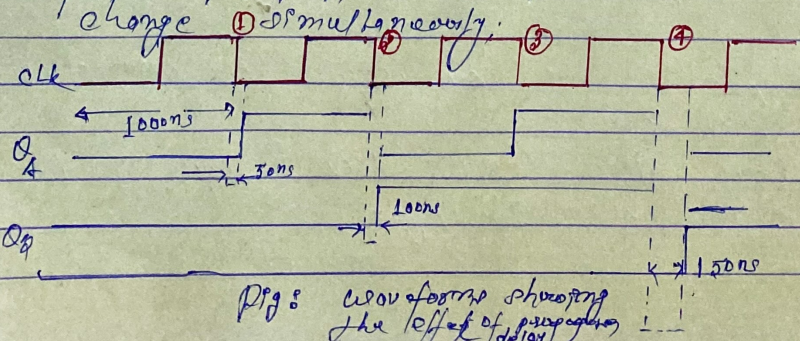


Fig: Waveforms showing the effect of propagation delay

In this diagram, the last diagram. FF's will take
3*50 = 450ns to change its state after the application
of 4th negative falling edge.